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EXAMINER

CHANG, RICK KILTAE

ART UNIT	PAPER NUMBER
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3729

DATE MAILED: 08/05/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/602,951

Applicant(s)

HABA, BELGACEM *an*

Examiner

Rick K. Chang

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-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 May 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) not recited in item 6 below is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-19,22,25-31,33 and 34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 8-9, 15-18 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al (US 6,098,282) in view of Larson (US 5,160,579).

Frankeny discloses an inner element (29) having first and second metal layers (26 and 36), through vias (34), a dielectric layer (40), and outer metal layers and another metal layer (Fig. 19), and all the claimed limitations.

Frankeny fails to disclose patterning the outer metal layers such that at least some of the metallic via liners are electrically isolated from the first and second metal layers. Frankeny fails to disclose coating the dielectric material to a thickness of approx. 25-75 or 25-50 microns, forming through vias before coating to a diameter of approx. 175-200 microns, forming through vias after coating to a diameter of approx. 25-150 microns, and forming metal layers to a thickness of approx. 1-18 microns.

Larson discloses patterning the outer metal layers such that at least some of the metallic via liners are electrically isolated from the first and second metal layers (Fig. 1K shows metal layers are etched to disconnect from the via liners).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Frankeny by patterning the outer metal layers such that at least some of the

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metallic via liners are electrically isolated from the first and second metal layers, as taught by Larson, for the purpose of preventing electrical communication between the first layer to the bottom layer.

At the time the invention was made, it would have been an obvious matter of design choice to a person of ordinary skill in the art to coat the dielectric material to a thickness of approx. 25-75 or 25-50 microns, form through vias before coating to a diameter of approx. 175-200 microns, form through vias after coating to a diameter of approx. 25-150 microns, and form metal layers to a thickness of approx. 1-18 microns because Applicants have not disclosed that coating the dielectric material to a thickness of approx. 25-75 or 25-50 microns, forming through vias before coating to a diameter of approx. 175-200 microns, forming through vias after coating to a diameter of approx. 25-150 microns, and forming metal layers to a thickness of approx. 1-18 microns provide an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicants' invention to perform equally well with the thickness and diameters as disclosed because it would give a fine pitch pattern printed circuit board without requiring expensive cameras or chemicals to form vias in the printed circuit board to communicate with inner metal layers, as well as electronic components mounted thereon.

Therefore, it would have been an obvious matter of design choice to modify Frankeny to obtain the invention as specified in claims 16, 18 and 26-27.

3. Claims 2, 4-7, and 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al (US 6,098,282)/Larson (US 5,160,579) as applied to claims 1, 8-9, 15, and 17 above, and further in view of Tsukada et al (US 6,378,201).

Frankeny/Larson selectively patterning the outer metal layers (Fig. 19), depositing a seed layer (9), plating a metal layer (42), simultaneously depositing metal layers to blind and through vias, and substantially all the claimed limitations, except for selectively etching the outer metal layers to form additional perpendicular signal lines and substantially parallel to the plane of the first and second metal layers.

Tsukada discloses selectively etching the outer metal layers to form additional perpendicular signal lines (40 and 40' above and vertical conductors in the blind vias) and substantially parallel to the plane of the first and second metal layers (Fig. 2I) thereby allowing the printed board to communicate with inner conductor layers and electronic components mounted thereon, as well as electrically communicate between the first layers to the bottom layers.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Frankeny/Larson by selectively etching the outer metal layers to form additional perpendicular signal lines and substantially parallel to the plane of the first and second metal layers to Frankeny/Larson printed circuit board, as taught by Tsukada, for the purpose of allowing the printed board to communicate with inner conductor layers and electronic components mounted thereon, as well as electrically communicate between the first layers to the bottom layers.

4. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al (US 6,098,282)/Larson (US 5,160,579)/Tsukada et al (US 6,378,201) as applied to claims 1 and 5 above, and further in view of Cziep et al (US 4,834,835).

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Frankeny/Larson/Tsukada fail to disclose plasma etching after the laser drilling the blind vias.

Cziep discloses plasma etching after the laser drilling (col. 3, lines 63-65 and col. 4, lines 15-16) thereby removing dielectric residues or deposits (col. 4, line 54).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Frankeny/Larson/Tsukada by plasma etching after the laser drilling the blind vias to Frankeny/Larson/Tsukada printed circuit board (PCB), as taught by Cziep, for the purpose of removing dielectric residues or deposits.

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al (US 6,098,282)/Larson (US 5,160,579) as applied to claims 1 above, and further in view of Ehrenberg et al (US 5,232,548).

Frankeny/Larson fail to disclose electrophoretically depositing the dielectric material.

Ehrenberg discloses electrophoretically depositing the dielectric material (col. 5, lines 9-10) thereby uniformly depositing the dielectric material without voids.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Frankeny/Larson by electrophoretically depositing the dielectric material of Frankeny/Larson PCB, as taught by Ehrenberg, for the purpose of uniformly depositing the dielectric material without voids.

6. Claims 22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al (US 6,098,282)/Larson (US 5,160,579) as applied to claims 1 above, and further in view of Official Notice.

Frankeny/Larson disclose etching the metal layers (col. 6, lines 43-45).

Frankeny/Larson fail to disclose laser drilling the inner dielectric element by using on of the metal layers as a mask.

Official Notice is taken that it is well known in the art to set a laser to a lower intensity to remove a dielectric material and align the laser to an opening formed in a metal layer (used as a mask) to drill holes in the dielectric element for the purpose of forming aligned openings without requiring expensive cameras.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Frankeny/Larson by laser drilling the inner dielectric element by using on of the metal layers as a mask to Frankeny/Larson PCB, as taught by Official Notice, for the purpose of forming aligned openings without requiring expensive cameras.

7. Claims 28 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al (US 6,098,282) in view of Larson (US 5,160,579), and further in view of DiStefano et al (US 6,274,820).

Frankeny discloses an inner element (29) having first and second metal layers (26 and 36), a through via (34), a dielectric layer (40), and outer metal layers and another metal layer (Fig. 19), and substantially all the claimed limitations.

Frankeny fails to disclose providing first and second metal layers having openings therein on opposite surfaces of the inner dielectric element and patterning the outer metal layers such that at least some of the metallic via liners are electrically isolated from the first and second metal layers.

Larson discloses patterning the outer metal layers such that at least some of the metallic via liners are electrically isolated from the first and second metal layers (Fig. 1K shows metal layers are etched to disconnect from the via liners).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Frankeny by patterning the outer metal layers such that at least some of the metallic via liners are electrically isolated from the first and second metal layers, as taught by Larson, for the purpose of preventing electrical communication between the first layer to the bottom layer.

DiStefano discloses providing first and second metal layers having openings therein on opposite surfaces of the inner dielectric element (Fig. 2) thereby utilizing the first and second metal layers as masks to form aligned openings in the dielectric layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Frankeny by providing first and second metal layers having openings therein on opposite surfaces of the inner dielectric element to Frankeny PCB, as taught by DiStefano, for the purpose of utilizing the first and second metal layers as masks to form aligned openings in the dielectric layer.

8. Claims 29 and 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frankeny et al (US 6,098,282)/Larson (US 5,160,579)/DiStefano et al (US 6,274,820) as applied to claim 28 above, and further in view of Tsukada et al (US 6,378,201).

Frankeny/Larson/DiStefano selectively patterning the outer metal layers (Fig. 19) and substantially all the claimed limitations, except for selectively etching the outer metal layers to form perpendicular signal lines.

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Tsukada discloses selectively etching the outer metal layers to form perpendicular signal lines (40 and 40' above and vertical conductors in the blind vias) thereby allowing the printed board to communicate with inner conductor layers and electronic components mounted thereon.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Frankeny/Larson/DiStefano by selectively etching the outer metal layers to form perpendicular signal lines to Frankeny/Larson/DiStefano PCB, as taught by Tsukada, for the purpose of allowing the printed board to communicate with inner conductor layers and electronic components mounted thereon.

Response to Arguments

9. Applicant's arguments with respect to claims 1, 2, 4-19, 22, 25-31, 33 and 34 have been considered but are moot in view of the new ground(s) of rejection.

Interviews After Final

10. Applicant note that an interview after a final rejection will not be granted unless the intended purpose and content of the interview is presented briefly, in writing (the agenda of the interview must be in writing) to clarify issues for appeal requiring only nominal further consideration. Interviews merely to restate arguments of record or to discuss new limitations will be denied. See MPEP 714.13 and 713.09.

Conclusion

11. Please provide reference numerals to all the claimed limitations as well as support in the disclosure for better clarity. Applicants are duly reminded that a full and proper response to this Office Action that includes any amendment to the claims and specification of the application as originally filed requires that the applicant point out the support for

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any amendment made to the disclosure, including the claims. See 37 CFR 1.111 and MPEP 2163.06.

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rick K. Chang whose telephone number is (703) 308-4784. The examiner can normally be reached on 5:30 AM to 1:30 PM, Monday through Friday, except for maxi-flex day off (any one of working days).

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9302 for regular communications and (703) 872-9303 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1148.

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A handwritten signature in black ink, consisting of stylized, cursive letters, positioned above a horizontal line.

RICHARD CHANG
PRIMARY EXAMINER

RC

July 23, 2003